

Yuanfang Hu

234 Escuela Ave. Apt. 56
Mountain View, CA 94040

Phone: 858-401-0027
Email: yhu@cs.ucsd.edu

Objective

Seeking a full-time software engineer position in web search, high performance computing, or related areas

Education

Ph.D. Computer Science, University of California, San Diego, 2007. GPA: 3.69/4.0

M.S., Computer Science, Tsinghua University, Beijing, China, 2000. GPA: 3.7/4.0

B.S., Computer Science, Tsinghua University, Beijing, China, 1998. GPA: 3.7/4.0

Skills

- Programming languages: Proficient in C/C++; good at Perl, Fortran, and Shell; familiar with SQL
- Operating systems: Linux, Unix (AIX, Solaris), Window XP/2000
- Tools: CVS, gdb, purify
- Experience in parallel computing, large-scale data management, computer architecture design and VLSI physical design
- Strong background in data structures and algorithms, strong problem solving skills
- Quick learner, good team player

Experience

11/2003 – present, Graduate Researcher, San Diego Supercomputer Center

- *Large-Scale Parallel Earthquake Simulation (Fortran, C / Linux)*
 - Developed a parallel earthquake simulation using MPI parallel programming, which runs on up to 2048 computer nodes, and generates over 50T scientific data
 - Used MPI I/O facilities to provide high storage performance on multi-processors
- *Data Management and Web Service for SRB Digital Library (PHP, Perl, Shell, C / Solaris)*
 - Developed web query interface to access large scale earthquake database
 - Managed large data sets (>100TB) in distributed digital library enabled by Storage Resource Broker (SRB)
 - Designed and implemented metadata management tool for SRB, which is able to automatically create, add, update, delete and display SRB metadata associated to files or directories.

9/2000 – present, Research Assistant, University of California, San Diego

- *Performance Driven Low Power Network-on-Chip Design (Ph.D. Thesis, C++ / Linux)*
 - Designed and implemented multicommodity flow models to improve communication power and latency of Network-on-Chip by 36-52%
 - Designed and implemented approximation algorithms and optimizations to efficiently solve large-scale multicommodity flow models
- *Dynamic Optimizer Design for VLIW Architecture (C++ / Linux)*
 - Designed and implemented an optimizer that dynamically optimizes loop instructions through software pipelining. Achieved an average of 12-16% speedup on a set of SPEC2000 benchmarks.

06/2003 – 09/2003, Intern, Programming Systems Lab, Intel Corp.

- *Compiler Automatic Parallelization Optimization (C++ / Linux)*
 - Analyzed and tested the auto parallelization optimizations in Intel's Open Research Compiler, including software pipelining, interprocedural analysis, etc.

09/1998 – 06/2000, Research Assistant, Tsinghua University, China

- *Integrated Configuration Software Development (Visual C++ / Windows)*

- Developed integrated configuration software in distributed control systems. Applied object-oriented methods to system design to achieve adaptability and reusability.

Publications

- **Y. Hu**, Y. Zhu, H. Chen, C.K. Cheng, “Communication Latency Aware Low Power Network-on-Chip Synthesis Through Topology Exploration and Wire Style Optimization”, *submitted to IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems*
- S. Zhou, Y. Zhu, **Y. Hu**, R. Graham, M. Hutton, C.K. Cheng, “Timing Model Reduction for Hierarchical Timing Analysis”, *International Conference on Computer Aided Design, 2006*
- **Y. Hu**, Y. Zhu, H. Chen, C.K. Cheng, “Communication Latency Aware Low Power NoC Synthesis”, *Design Automation Conference, 2006*
- **Y. Hu**, H. Chen, Y. Zhu, A. A. Chien, C.K. Cheng, “Physical Synthesis of Energy-Efficient NoCs Through Topology Exploration and Wire Style Optimization”, *International Conference on Computer Design, 2005*
- J. Weinberg, A. Jagatheesan, A. Ding, M. Faerman, **Y. Hu**. “Gridflow Description, Query, and Execution at SCEC using the SDSC Matrix”, *International Symposium on High-Performance Distributed Computing, 2004*
- S. Narayanasamy, **Y. Hu**, S. Sair, B. Calder. “An Instruction Scheduling Co-Processor for Adaptive VLIW Schedules”, *International Conference on High Performance Computer Architecture, 2004*
- S. Sair, **Y. Hu**, T. Sherwood, B. Calder. “Optimized Trace Binaries for Architectural Evaluation”, *UCSD Technical report CS2002-0711, 2002*
- **Y. Hu**, S. Zhang, W. Jiang. “Applying Object-Oriented Method to CSIE System”, *International Conference on Technology on Object-Oriented Languages and Systems, 1999*

References

Available upon request